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Ultra-low power 0.45 mW 2.4 GHz CMOS low noise amplifier for wireless sensor networks using 0.13-µm technology

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ABSTRACT

This paper describes the design topology of a ultra-low power low noise amplifier (LNA) for wireless sensor network (WSN) application. The proposed design of ultra-low power 2.4 GHz CMOS LNA is implemented using 0.13-µm Silterra technology. The LNA benefits of low power from forward body bias technique for first and second stages. Two stages are implemented in order to enhance the gain while obtaining low power consumption for overall circuit. The simulation results show that the total power consumed is only 0.45 mW at low supply voltage of 0.55 V. The power consumption is decreased about 36% as compared with the previous work. A gain of 15.1 dB, noise figure (NF) of 5.9 dB and input third order intercept point (IIP3) of -2 dBm are achieved. The input return loss (S11) and the output return loss (S22) is -17.6 dB and -12.3 dB, respectively. Meanwhile, the calculated figure of merit (FOM) is 7.19 mW^{-1}.

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1. INTRODUCTION

A wireless sensor network (WSN) develops very fast in the market because it offers great functions. The WSN has basic specifications such as the accuracy, flexibility, reliability, expenses, power consumptions and the difficulty of designing [1]. Part of that, the power consumption is the most important specification due to the battery powered of the nodes [2]. Consequently, this specification leads to a great development of CMOS RF usage in a research area. The reasons are due to the low cost and size which are capable to be fabricated on a single chip and can be integrated in many applications [3].

In the front-end of the RF receiver chain, LNA is a block that cannot be replaced [4-6]. The functions of LNA are to boost the signal received from the receiving antenna and transmit the signal with high gain to minimize noise contribution of the next stages [7, 8]. There are many publications of CMOS LNAs focusing on gain [9-11]. However, only a few recent published works are related to the very low power LNA. In [12], the topology of a two-stage cross-coupling cascaded common gate (CG) is adapted by using 0.18 µm TSMC process. It achieves gain of 16.8 dB and power consumption of 2.16 mW. But the inductor is fabricated separately with a large value which is 32 nH. Besides, by using a current-reused topology can also obtain low power consumption [13]. It achieves gain of 14 dB and 2.45 mW. The proposed design uses a few inductors and consequently increases the chip size.

Hence, the aim of this work is to design a LNA with low power consumption and other specification within the expectation range. The power dissipation of the LNA must be minimized in order to extend the battery lifetime of the wireless sensor nodes [14]. Therefore, a design based on forward body bias with two stages is presented [15]. In order to reduce power consumption, forward body bias is an effective technique. This is because it will lower down the supply voltage by decreasing the threshold voltage and thus the power consumption can be reduced [15-17]. The dc bias at the bulk terminal of transistor can be varied to control the threshold voltage [18]. The similar work has been presented in [7]. However, the second stage is not connected correctly as a cascade topology. Therefore, the simulation results are questionable. The proposed work also performed pre-layout simulation results without the layout. This paper is organized as follows: in Section 2, the forward body bias technique is explained, the proposed LNA circuit design is analyzed in Section 3. Section 4 presents the simulation results achieved from the proposed circuit design and finally, Section 5 concludes overall achievement.

2. FORWARD BODY BIAS TECHNIQUE

Due to the simplicity of the forward body bias technique; it is used in this topology as to lower down the value of power consumption of the LNA [15] which will be discussed in details as below. This topology of LNA is implemented and designed by using a 0.18-µm CMOS technology [15]. The LNA operates at 2.4 GHz with only 0.6 V of supply voltage and achieves 2.88 dB of NF, 10.1 dB of gain, and power consumption is 0.84 mW. Figure 1 shows the schematic of the forward body bias topology. Typically, the equation between the threshold voltage and the body-source voltage is given as [16].

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_f - V_{bs}} - \sqrt{2\phi_f}) \quad (1)$$

where V_{tho} is the threshold voltage for V_{bs} = 0, γ is a process-dependent parameter, ϕ_f is a semiconductor parameter with a typical value in the range of 0.3-0.4 V, V_{bs} is the source-to-body voltage. From Figure 2, it can be seen that the V_{th} is decreased when V_{bs} is increased. Therefore, the low voltage and low power LNA can be achieved in the design without affecting other device characteristics of gain, linearity and noise figure [15]. The forward body bias technique has low linearity inherently but can be done with simplicity which resulted to a smaller size of the LNA.

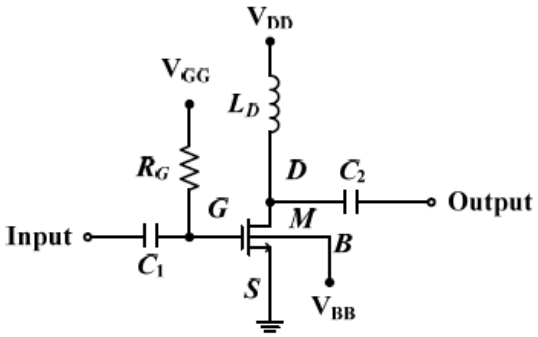

Figure 1. The schematic design of two stages LNA

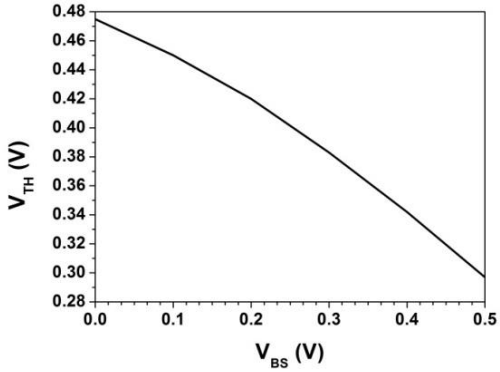

Figure 2. The calculated threshold voltage of NMOS when varying V_{BS} from 0 to 0.5V [19]

3. LNA CIRCUIT DESIGN

The design approached is based on previous published technique which is forward body bias [14] and single forward body bias technique [19-20]. The proposed LNA is shown in Figure 3. The technique is employed forward body bias technique for both stages. This LNA operates at low supply voltage which is 0.55 V. The cascode structure is employed in the first stage and the second stage which consist of transistor M1, M2 and M3, M4, respectively. The suitable sizes for transistors are chosen as to ensure an acceptable gain at low bias voltage. The size of M1 and M2 is set to 130 µm/0.13 µm with 13 fingers and 10 µm widths while the size of M3 and M4 is set to 120 µm/0.13 µm with 12 fingers and 10 µm widths. The bulk voltage (VB) of M1, M2, M3 and M4 is 0.3 V through R4 is chosen in order to ensure that the transistors operate

in a saturation region. The inductor L1 affects input matching and also input stage gain. Moreover, the inductor L1 and capacitor C1 provides DC path for transistor M1. Capacitor C2 is resonates with L2 as to improve a gain and an input matching while to guarantee that the design operate at frequency 2.4 GHz. A C5 provides DC path to the next stage of the LNA design.

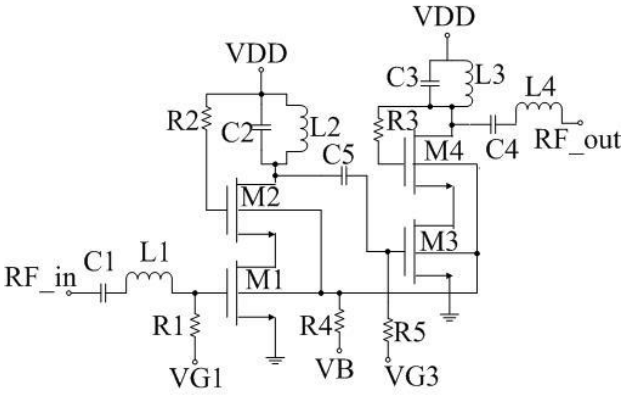

Figure 3. The schematic design of two stages LNA

4. SIMULATION RESULTS

In order to generate S-parameters, noise figure, stability and linearity, the simulations are carried out using the Cadence Spectre analog design environment (ADE). Hence, the simulated results that are obtained from two stages forward body bias technique at 2.4 GHz are presented in this section. The overall circuit operates at 0.55 V supply voltage and draws 820 µA of the total current. The pre-layout and post-layout results of S11 are illustrated in Figure 4. The input return loss, S11 for pre-layout is -23.2 dB while for post-layout is -17.6 dB at 2.4 GHz. From the Figure 2, it can be seen that both pre-layout and post-layout results are agreed to each other. The differences is due to the extracted parasitic that exists during the simulation has affected the input matching of the LNA [14]. But, the value is still in the acceptable range. Figure 5 depicts the output return loss (S22) of the proposed two stages LNA. It can be seen that both the pre-layout and the post-layout are -16.6 dB and -12.29 dB respectively. As can be seen in Figure 5, the post-layout curve is shifts to the right from the operating frequency, 2.4 GHz. This happens due to the parasitic of routing, capacitance, inductance and output pad.

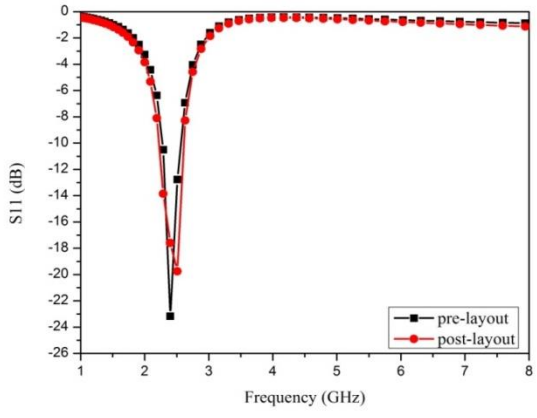

Figure 4. The input return loss (S11) of two stages LNA

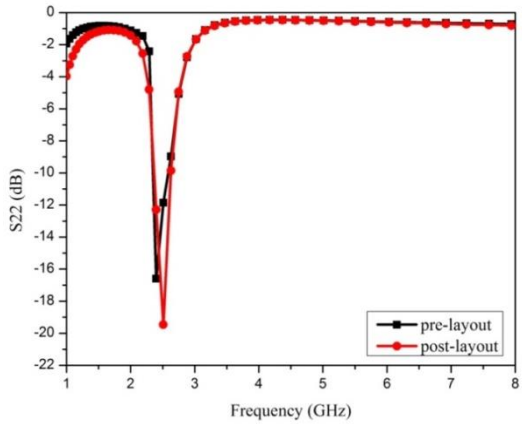

Figure 5. The output return loss (S22) of two stages LNA

Figure 6 depicts the voltage gain (S21) of the proposed two stages forward body bias with cascode configurations LNA. From the pre-layout simulation results, the peak voltage gain, S21 of 19.71 dB

is observed for overall circuit. But, the gain is degrading to 15.05 dB during post-layout simulation. The reason is because of the existence of the extracted parasitic in load inductors. Figure 7 illustrates the pre-layout and post-layout simulations results for the noise figure (NF). The NF of 4.9 dB and 5.9 dB is achieved for the pre-layout and post-layout at 2.4 GHz, respectively. The increasing of NF is due to the parasitic effects. Moreover, the transmission lines from the input pad to the inductor and gate of transistor can be modelled by a resistor which can also contribute to the noise. In addition, there are more components for the proposed two stages LNA which can also contribute to the noise for overall performance. However, the NF achieved from this LNA circuit is within the specifications performance.

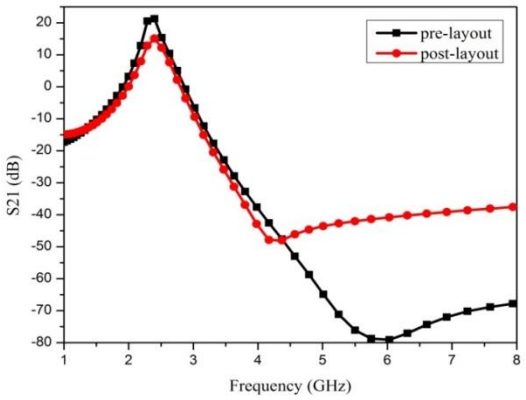

Figure 6. The voltage gain (S21) of two stages LNA

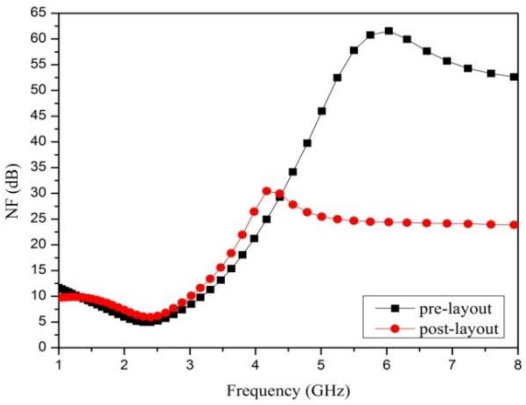

Figure 7. Noise Figure of the proposed LNA

Linearity is performed as it can determine the performances of the LNA. It occurs when an unwanted signal presents nearer to the operating frequency. The higher linearity is more desirable. First, the linearity of the proposed LNA is simulated by the input 1 dB compression point (IP1dB). As illustrates in Figure 8, the simulated IP1dB of -15 dBm is obtained at 2.4 GHz. Meanwhile, the third-order intercept point (IIP3) is the interception of the first-order output curve and the third-order intermodulation output curve at 2.4 GHz is shown in Figure 9. As can be seen in Figure 9, the IIP3 for the proposed two stages LNA of -2 dBm is achieved. The stability factor from the proposed LNA which is more than one is achieved as shown in Figure 10. Therefore, the proposed LNA is unconditional stable.

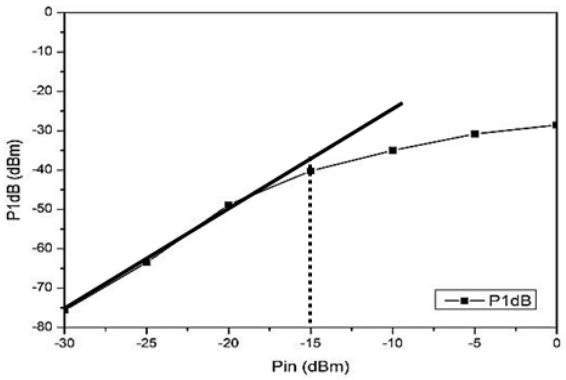

Figure 8. Noise Figure of the proposed LNA

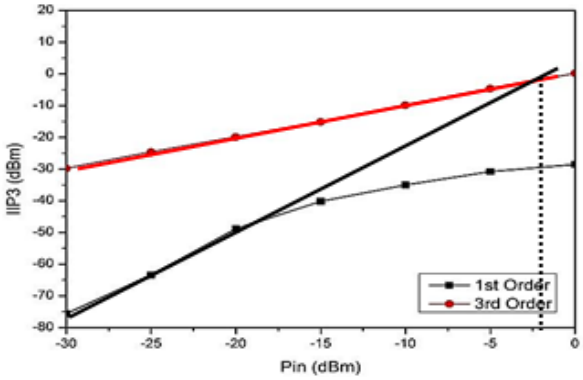

Figure 9. Simulated result of IIP3 of two stages LNA

The layout of the proposed two stages LNA is illustrated in Figure 11. All components are designed on-chip. In the layout, spiral inductors and metal-insulator-metal (MIM) capacitors are used due to high quality factor and low losses, respectively. The total layout area is 0.99 mm × 0.98 mm which consists of two GSG pads, three dc pads, four inductors, DC block, five capacitors, four RF resistors and four transistors. The layout will be tape out in the future.

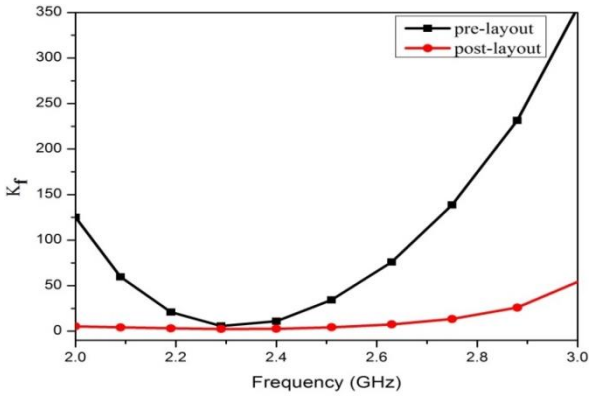

Figure 10. Stability of the proposed two stages LNA

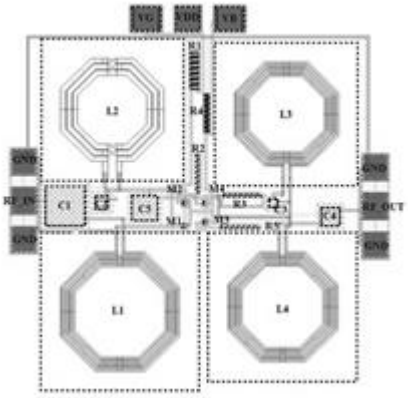

Figure 11. The layout of the proposed two stages LNA

The overall post-layout results performances comparison between the proposed LNA with recently published works is summarized in Table 1. This proposed LNA consumes only 0.45 mW for overall circuit with 0.55 V supply voltage. The LNA cannot be replace or remove in the RF receiver front-end [21]. Therefore, it should deliver a significant gain to minimize the noise contribution of the subsequent stages and to amplify the attenuated signal received by the antenna so that it can be efficiently handled by the next stages such as mixer and VGA [4]. A low voltage and low power LNA's performance is evaluated based on figures of merits (FOMs). There are different FOMs are commonly used in the previous works [22]. One of the FOM of the LNA can be calculated based on the ration of power gain to the power dissipation and NF performance as represented in (2).

$$FOM\ [\mathrm{mW}^{-1}] = \frac{Gain_{(abs)}}{(NF-1)_{(abs)} \times P_{DC}} \quad (2)$$

where, *abs* is the absolute value of gain and NF [23]. Comparing with the other works, the proposed LNA obtains the lowest power consumption. Besides, the linearity performance of this work is better than others. Meanwhile, gain is comparable by considering a low supply voltage. Referring to [21], high gain and good FOM are achieved without linearity (IIP3) performance. References [24] also obtained high gain with high power consumption. Based on the calculated FOMs in Table 1, the proposed LNA shows the best performances than other proposed LNAs.

Table 1. Overall performances comparison of the proposed LNA (post-lyout)

Parameter	[13]	[21]	[24]	[25]	This work
CMOS Technology (µm)	0.13-µm	0.18-µm	0.18-µm	0.18-µm	0.13-µm
Supply Voltage (V)	0.8	1.2	1.8	1.0	0.55
Frequency (GHz)	3.7	2.4	2.4	2.4	2.4
Gain (dB)	14	20	20.10	18.2	15.1
S11, S22 (dB)	-10.6, N/A	<-13.5, N/A	N/A	N/A	-17.6,-12.3
NF (dB)	2.0	5.6	3.2	3.4	5.9
IP1dB (dBm)	N/A	N/A	N/A	-15	-15
IIP3 (dBm)	10.5	N/A	-2.4	-4.32	-2.0
Power (mW)	2.45	0.70	1.30	0.97	0.45
FOM (mW^{-1})	1.82	8.41	6.04	6.37	7.19
Chip Size (mm^2)	N/A	0.02	0.03	0.04	0.97

5. CONCLUSION

A very low power 2.4 GHz two stages CMOS LNA using forward body bias technique has been proposed in this work. As the forward body bias technique allows for the reduction of the threshold voltage and thus reduces the power consumption, therefore the technique was implemented in this work. Two stages LNA is proposed as to enhance the overall gain. In order to get low power consumption, this circuit

is designed which capable to operate at a low supply voltage which is 0.55 V. The post-layout results show that the power consumption of 0.45 mW is obtained with the FOM of 7.19 mW^{-1}. The power consumption is decreased about 36% as compared with the previous work. The overall chip size is 0.97 mm^2. The simulation results validate peak performance at 2.4 GHz that suitable for wireless sensor network applications.

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